4x8 RF Switch Matrix

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Current document represents technical data for solid state 4x8 RF switch matrix. Device enables very high test equipment utilization by switching RF routes between four (4) instrument and eight (8) Device Under Test (DUT).

Features and advantages:
- Enables reducing test time per DUT by high speed RF route switching between multiply test instruments and DUT’s.
- Maintenance free, no limitation for switching cycles
- Based on high-end UltraCMOS technology
- Broadband coverage from 1MHz up to 6.0 GHz
- High switching speed
- High isolation and low VSWR
- Unused RF ports are internally terminated into 50Ω
- RF and control routes are ESD protected
- Enable 3.3V or 5V control

Absolute maximum ratings:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency range</td>
<td>10MHz</td>
<td>6GHz</td>
</tr>
<tr>
<td>Operating voltage, Vdd</td>
<td>3.2V</td>
<td>5.5V</td>
</tr>
<tr>
<td>Control voltage, Vctrl</td>
<td>3.2V</td>
<td>5.5V</td>
</tr>
<tr>
<td>RF input power for active RF route</td>
<td>+27 dBm @10-50MHz</td>
<td>+30 dBm @50-400MHz</td>
</tr>
<tr>
<td>RF input power for unused port (to internal termination)</td>
<td>+24 dBm @10MHz-6GHz</td>
<td></td>
</tr>
<tr>
<td>Hot switching: allowed but not recommended</td>
<td>24dBm max</td>
<td></td>
</tr>
<tr>
<td>Operating tem.</td>
<td>-10°C</td>
<td>+65°C</td>
</tr>
</tbody>
</table>

Technical specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>10MHz-0.7GHz</th>
<th>0.7-4.0 GHz</th>
<th>4.0-6.0GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input impedance</td>
<td>50 ohm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insertion loss max.</td>
<td>5.5 dB</td>
<td>8.0 dB</td>
<td>9.0dB</td>
</tr>
<tr>
<td>Return Loss min.</td>
<td>17dB</td>
<td>20dB</td>
<td>15dB</td>
</tr>
<tr>
<td>Isolation between used and unused port</td>
<td>&gt;50 dB</td>
<td>&gt;40 dB</td>
<td>&gt;35 dB</td>
</tr>
<tr>
<td>Input 1dB compression, typ</td>
<td>+26 dBm</td>
<td>+33 dBm</td>
<td>+33 dBm</td>
</tr>
<tr>
<td>Input IP3, typ</td>
<td>+56dBm</td>
<td>+60dBm</td>
<td>+60dBm</td>
</tr>
<tr>
<td>Switching time</td>
<td>&lt;20μsec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF connectors, Port A1 - A4</td>
<td>4xN-female</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF connectors, Port B1 – B8</td>
<td>8x SMA-female</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTRL connector</td>
<td>DIN 41651, 50-pin PCB angled male connector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC connector</td>
<td>Phoenix contact, 3-pin PCB angled connector, 3.5mm pitch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case dimensions</td>
<td>120x150x22mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RF diagram
Control and DC connection diagram
Switch matrix consists of two RF relay arrays A of size 4 and B of size 8. Relays of arrays A and B must be addressed in such a way that signal path of relays pointed to each other must meet in between. For example if port A[2] is to be connected to port B[5], then relay cluster of port A[2] must address destination of port B[5] and accordingly relays of port B[5] must address port A[2]. If we primary select port A destination then address of the port B could be calculated from expression:

\[
\text{for } i := 0 \text{ to } 3 \text{ do}
\begin{align*}
  Bsel[i] & := i; \\
\end{align*}
\]

where Asel and Bsel are selection addresses of port relay matrixes A and B accordingly.

There must be noted that with asymmetric matrix 4 x 8, four of B ports will remain unconnected, but still must (are) be pointed to some of the A ports. Careful selection of this destination could improve isolation of valid connections. Since destination range of port A is 0 to 7 then 3 bit address is applied to the each of 4 A port relay matrixes.

Control lines of A ports are connected as:

- A[0].0 – pin 32
- A[0].1 – pin 31
- A[0].2 – pin 30
- A[1].0 – pin 24
- A[1].1 – pin 23
- A[1].2 – pin 22
- A[2].0 – pin 16
- A[2].1 – pin 15
- A[3].0 – pin 8
- A[3].1 – pin 7
- A[3].2 – pin 6

Accordingly each of 8 ports B relay matrixes address one of 4 ports A and each has 2 bit address connected as:

- B[0].0 – pin 40
- B[0].1 – pin 39
- B[1].0 – pin 38
- B[1].1 – pin 37
- B[2].0 – pin 36
- B[2].1 – pin 35
- B[3].0 – pin 34
- B[3].1 – pin 33
- B[4].0 – pin 48
- B[4].1 – pin 47
- B[5].0 – pin 46
- B[5].1 – pin 45
- B[6].0 – pin 42
- B[6].1 – pin 43
- B[7].0 – pin 42
- B[7].1 – pin 41

Pins 49 and 50 are connected to the common ground.

There are LVC technology buffers on each connector input pin to protect relays from static electricity and incorrect input voltages.

Better solution would be internal controller performing all needed address calculation tasks and interfaced from outside just by USB connector. In this case the power could be also derived from USB line.
Measured RF characteristics